Forward with Active Clamp for space applications: clamp capacitor, dynamic specifications and EMI filter impact on the power stage design

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***Abstract*—The impact of the clamp capacitor design, the dynamic specifications and the EMI filter design on the power stage design of a 28V 50W Forward with Active Clamp converter for space applications is analyzed along this paper. Clamp capacitor is designed by considering the ECSS standards limitations for the semiconductors and saturation of the magnetic components, and considering the influence of the resonance between this capacitance and the magnetizing inductance on the input impedance of the converter. Dynamic specifications influence are analyzed. Additionally, the EMI filter design process is described. Single-stage and Multi-stage approaches are proposed. All these features make an increase of 2.4W losses and 1.6 higher area of the converter, compared with a preliminary design of the power stage, before considering these aspects.**

I. Introduction

The first step to design any power converter is to analyze different topologies and compare them in terms of losses, size and performance. One of the most common ways to do a first approach is to provide a preliminary choice of the semiconductors devices, capacitors and magnetic components and then calculate their corresponding losses, thus obtaining a first design of the power stage. However, these are not the only features that shall be considered in order to get a final design. There are other constraints and specifications, related to the dynamic response, the EMI limitations and some particular issues from each topology, that might require some modifications on the power stage, specially for aerospace applications, for which robustness and reliability make these requirements stronger than for other kind of industrial applications.

Along this paper, a further analysis of these issues for a 50W 28V Forward with Active Clamp (Figure 1) for space applications is analyzed, which is more detailed in [1]. The preliminary power stage is developed in [2], where semiconductors, magnetic components and output capacitors are given.

For this particular topology, clamp capacitor is one of the most important features to analyze before closing a final design of the power stage, because it influences the ripple of the primary voltage, that might affect the choice of the semiconductor devices or the size of the magnetic components, as well as the minimum input impedance of the converter, which is crucial for the design of the EMI filter. Additionally, its dynamic behavior shall be analyzed in order to avoid problems related with the saturation of the transformer. By considering these aspects, the dynamic specifications and the EMI filter, an increase of almost 60% of the area of the converter and a reduction of a 4% of the efficiency are the consequence, what shows the importance of studying these aspects in order to provide a final design of the power stage.

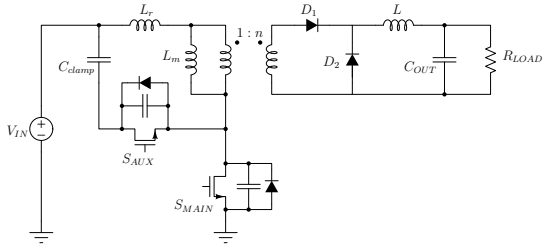

Fig. 1. Forward with Active Clamp.

Table I shows the main general specifications for the analyzed converter. Some different conditions for power, input voltage and load steps are made for nominal and transient situations. Additionally, the design shall be able to operate with up to four converters of the same power in parallel. This condition has a strong impact on the EMI filter design, as explained later.

TABLE I
General specifications for the converter.

	Nominal	Transient
Output power	50W	76W
Input Voltage	18V to 38V	13.5V to 55V
Load steps	2.7A to $10mA$	$825mA$ to $10mA$
Paralleling	Up to 4 modules	
Control	*Peak Current Mode Control*	

II. Active clamp: clamp capacitor design

Active Clamp technique is a method to demagnetize the core of the transformer of some DC/DC converters with reduced losses and avoiding the use of other classical techniques like adding an extra winding to provide a path to demagnetize the core. This technique is applied to the Forward converter in [3], [4] y [5]. A proper selection of the clamp capacitor, C_{cl}, is required in order to avoid exceeding the breakdown voltages of the switching devices or the flux density saturation of the transformer, due to its ripple. It is specially important for space applications, in which certain deratings shall be applied according to some regulations, such the ECSS Standards. Additionally, there is a resonance between the clamp capacitor and the magnetizing inductance that strongly influences the input impedance of the converter, thus constraining the design of the EMI filter, as explained later.

A. Clamp voltage ripple

In order to keep the same semiconductor devices and magnetic components that were designed for the preliminary power stage design, voltage ripple in the clamp capacitor needs to be considered, since it is reflected on the drain-to-source voltages and therefore on the voltage applied to the primary of the transformer.

Voltage ripple in the clamp capacitor is described as:

$$\Delta V_{cl} = \left.\frac{\int idt}{C_{cl}}\right|_{T_s} = \frac{(i_{Lm_{pk-pk}} - \frac{V_{cl}(1-D)T_{sw}}{L_m}) \cdot (1-D) \cdot T_{sw}}{2 \cdot C_{cl}} \tag{1}$$

Where L_m is the magnetizing inductance, C_{cl} is the clamp capacitance, $i_{Lm_{pk-pk}}$ is the peak to peak magnetizing current, D is the duty cycle, T_{sw} is the switching period and V_{cl} is the steady-state level of the clamp voltage, that is defined in terms of the output voltage, the duty cycle and the turns ratio ($n = \frac{n_{sec}}{n_{pri}}$):

$$V_{cl} = V_{in} \cdot \frac{D}{1-D} = \frac{V_{out}}{n \cdot (1-D)} \tag{2}$$

According to the ECSS standards, a 50% derating must be considered for the breakdown voltage of the MOSFETs, V_{BDSS}, what means that maximum drain-to-source voltage in the circuit shall not reach the 50% of the breakdown level. Then, next condition can be established in order to get the needed minimum clamp capacitance:

$$V_{BDSS} > \left.\frac{1}{derating(\%/100)} \cdot (V_{in} + V_{cl} + \Delta V_{cl})\right|_{MAX} \tag{3}$$

Clamp capacitor must be higher than $40n$F in this case. Otherwise,a lower capacitance would lead to use semiconductor devices with higher maximum ratings, thus worsening the losses of the converter.

Additionally, clamp capacitor voltage ripple also affects to the voltage applied to the transformer, so it shall be considered in order to calculate the maximum magnetic flux density:

$$B_{max} = (V_{cl} + \frac{\Delta V_{cl}}{2}) \cdot \left.\frac{(1-D) \cdot T_{sw}}{2 \cdot N_{pri} \cdot A_e}\right|_{V_{cl}=V_{cl_{max}}} \tag{4}$$

Where A_e is the effective area of the core and N_{pri} is the number of turns in primary. In a similar way to the previous constraint, a 60% derating needs to be applied (maximum flux density shall not exceed the 60% of the saturation level, B_{sat}).

$$B_{sat} > \left.\frac{1}{derating(\%/100)} \cdot B_{max}\right|_{V_{cl}=V_{cl_{max}}} \tag{5}$$

With this constraint, a minimum clamp capacitance of $24n$F is obtained, which is less restrictive than the previous condition. Then, $40n$F is set as the minimum required. According to both statements, a higher capacitance is preferable in order to reduce the ripple. However, there are other implications of the clamp capacitor that must be analyzed.

B. $L_m - C_{cl}$ resonance: influence on the input impedance

The resonance between magnetizing inductance and clamp capacitor influences the input impedance of the converter. Therefore, the choice of C_{cl} also affects the design of the EMI filter.

Resonant frequency of the clamp network depends on the input voltage (and then on duty cycle), because magnetizing current only flows through the clamp capacitor during $(1-D) \cdot T_{sw}$ (when the main switch is off). It is defined as:

$$f_{clamp} = \frac{1-D}{2\pi \cdot \sqrt{L_m \cdot C_{cl}}} \tag{6}$$

Fixing this resonant frequency at higher frequencies than bandwidth of the system is recommended when MOSFET current is sensed and used as control variable, since the resonance is reflected in the current gain transfer function and then in the loop gain of the system. A lower clamp capacitance value would be required in this case, what is opposite to the last condition.

On the other hand, a higher capacitance will lead to a less impedance restrictive EMI filter, because the characteristic impedance, Z_{Ch}, of the $L_m - C_{cl}$ is defined as:

$$Z_{Ch} = \sqrt{\frac{L_m}{C_{cl}}} \tag{7}$$

Furthermore, with the absence of parasitic resistances, the impedance of the $L_m - C_{cl}$ network would tend to infinite. As a consequence, the input impedance of the converter would go to low values at the clamp resonant frequency, thus making more restrictive the EMI filter design. A damping resistor is then required in order to decrease this effect. A common choice for this resistor is to set it at the characteristic impedance value of the clamp network. Losses in this resistor shall be considered. Table II shows the corresponding losses in the damping resistor for some particular values of the clamp capacitor, with an $L_m = 340\mu$F. The higher the C_{cl} the lower

the losses. However, the choice of the C_{cl} will depend on other dynamic constraints, explained along next section.

It is essential for space applications to assure a proper operation even in *Worst Case Conditions*, what means that all tolerances of the components, due either to aging, radiation or temperature effects, shall be considered into the design process. It is important to analyze the variation on the input impedance made by tolerances of the $C_{cl} - L_m$ ($\pm 30\%$ for C_{cl}, $+6\% - 36\%$ for L_m). The most restrictive case is the minimum voltage at high load, for which the input impedance is smaller as current at the input is higher. The *Montecarlo Analysis* tool from *SIMetrix-SIMPLIS* software has been used in order to compute all possible solutions for input impedance of the converter. For the particular case where $L_m = 340\mu$F, $C_{cl} = 450n$F and $R_{damp} = 20\Omega$, results of this analysis are shown in Figure 2. It can be seen that there is a huge variation on the input impedance, specially at the clamp resonant frequency (between $2.5k$Hz and $5k$Hz) and at $50k$Hz, which corresponds to the half of the switching frequency, that is due to the effect of the compensation ramp. This will need to be considered in the EMI filter design.

TABLE II
LOSSES IN DAMPING RESISTOR.

C_{cl}	R_{damp}	P_{damp}
$40n$F	92Ω	$590m$W
$470n$F	27Ω	$170m$W
4.7μF	9Ω	$54m$W

III. DYNAMIC CONSTRAINTS INFLUENCE

The preliminary design of the power stage only considers steady-state conditions. However, there are some dynamic constraints, related to output voltage deviation and saturation of the magnetic components under load steps, that may require changes on the power stage and need to be analyzed.

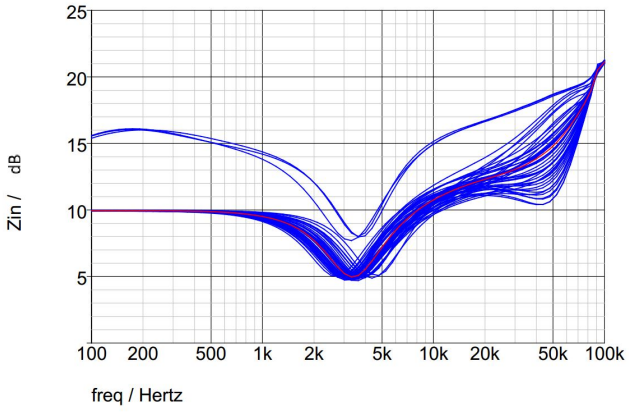

Fig. 2. *Montecarlo* analysis of the input impedance of the converter at $V_{in} = 18$V and maximum load ($I_{out} = 2.7$A). Nominal case in red, worst case analysis in blue.

A. Output voltage deviation under load steps

The first approach to design the output capacitors only considers the maximum allowed voltage ripple (500mV) and the *RMS* current that they need to stand (472mA, after applying 70% derating). As a result, 2 capacitors KEMET-T541 of 63V 10μF were selected (total output capacitance of 20μF).

But there is a constraint that shall be fulfilled: the maximum allowed output voltage deviation under a load step. For this project, $\Delta V_{out} = 500$mV deviation is allowed under a load step from 1.75A to 10mA and opposite ($\Delta I_{out} = 1.74$A). Then the required output capacitance can be estimated as follows:

$$C_{out} > \frac{1}{2\pi \cdot f_{BW} \cdot R_{eq}} = \frac{\Delta I_{out}}{2\pi \cdot f_{BW} \cdot \Delta V_{out}} \tag{8}$$

Where f_{BW} is the bandwidth frequency, 10kHz in this case. As a result, the new output capacitance must be higher than 55μF, so 6 capacitors KEMET-T541 63V 10μF are chosen (total output capacitance of 60μF).

It can be seen that the impact of this constraint leads to an output capacitor three times bigger (in terms of capacitance and volume) than the required for the preliminary design.

B. Effect of the clamp capacitor under load steps

Clamp capacitor has a strong impact on the dynamic response of the converter. The charging/discharging time of this capacitor makes a variation on the magnetizing current under a load step. Even if the transformer was properly designed according to the power stage conditions, that effect may cause the saturation of the core. To minimize this effect, some changes on the power stage can be done, as modifying the clamp capacitor and the core size of the transformer.

1) Clamp capacitance value:

Regarding the previous constraints, a minimum value of $40n$F is required for the clamp capacitor. A higher clamp capacitance is useful in order to reduce the voltage ripple and also it leads to set the resonance with the magnetizing inductance at lower frequency, what is a benefit for the EMI filter design. However, there is a limitation on the maximum value for this capacitor, due to the dynamic behavior during a load step. Then, there is a trade-off to choose this capacitor.

Figure 3 shows the difference between a $4.7\mu F$ and a $470n$F (which shows a compromise between ripple and the time constant) clamp capacitors during a load step from $100m$A to 2.7A. *Peak Current Mode Control (PCMC)* and a basic model for the transformer (with L_m and L_{lk}) are used for this test. The 4.7μF capacitor has a time constant around one hundred times higher than $470nF$. As a consequence, the voltage in the clamp capacitor needs more time to reach its new steady-stage value. Along this time, it can be seen that the DC value of the magnetizing current starts increasing, thus reaching the saturation of the core ($770m$A) during more than 10 cycles. This is because the clamp voltage, V_{cl}, has not reached its steady-state value, so it is not enough to demagnetize the core until that moment. With a real saturable transformer, this saturation of the core will lead to high spikes on the

primary current, which is not controlled. As a consequence, the clamp voltage would fast increase and might break the clamp capacitor.

On the other hand, with a $470nF$ capacitor, the time constant is smaller and then the maximum magnetic flux is reduced. Then, $470nF$ capacitor is more appropriate. However, it still saturates during three cycles, so some additional changes must be done to avoid this saturation.

2) Core size of the transformer:

The core size of the transformer can be increased in order to increase the saturation level. With an RM8/I, the saturation current is $770mA$, it increases to $910mA$ by using and RM10/I. Then, for this particular case, using an RM10/I core is useful to avoid the saturation problems under the specified load steps.

IV. EMI FILTER DESIGN

Additionally, an EMI filter is required in order to limit the noise injected into the source and to assure a good quality of the input of the converter. The addition of this EMI filter increases the volume and losses of the converter, compared with the preliminary power stage design. The design limitations and different filter structures are described next.

A. Constraints and specifications

The main requirement of an EMI filter is to attenuate the switching harmonics to meet the conducted electromagnetic interference regulation limits. Stability of the system must be assured under all conditions. Maximum used capacitance in the filter is also constraint for this particular project.

1) Conducted emission limit: Conducted emission in differential mode injected by the converter in the primary bus is always under some limitations. Figure 4 shows the regulation applied to this project. Red line limit is applied for nominal values of the components under nominal conditions. On the other hand, blue line show the limit for worst case analysis in which tolerances and transient conditions are analyzed.

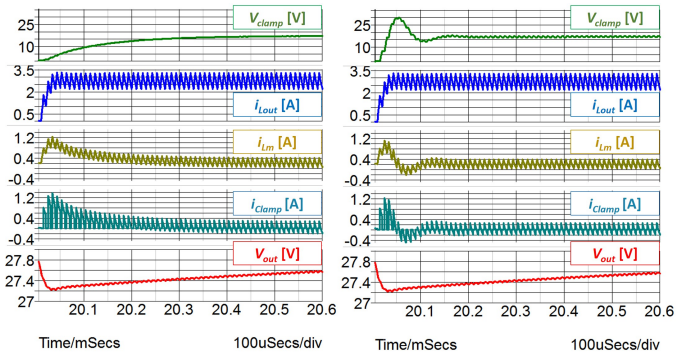

Fig. 3. Influence of the clamp capacitance value. Ideal model of the transformer (RM8/I) is used. $C_{clamp} = 4.7\mu F$ *on the left,* $C_{clamp} = 470nF$ *on the right. From top to bottom:* $V_{clamp}, i_{L_{out}}, i_{Lm}, i_{Clamp}, V_{out}$

Therefore, the input current spectrum needs to be analyzed for the worst case (at the highest input current and regarding tolerances of the components). Usually harmonic at the switching frequency is the most restrictive. Needed attenuation is then calculated in order to filter enough this harmonic so that it is below the regulation mask. -67.2dB under nominal conditions and -61.2dB for worst case are required in this project. This will give a minimum $L-C$ product, as attenuation is described as:

$$Att_{dB} = 20 \cdot log(\frac{1}{L_f \cdot C_f \cdot (2\pi \cdot f_{att})^2}) \tag{9}$$

2) Middlebrook's criteria: stability: As explained in [8], stability is assured if a $6dB$ margin is kept between the output impedance of the filter and the input impedance of the converter. However, this condition might sometimes be too much conservative. A $6dB$ margin has then considered for nominal conditions and $3dB$ for worst case conditions. It is important to highlight that up to four converters must be able to work in this particular project, what affects the stability conditions. Figure 5 shows the worst case analysis obtained results with the final Multi-stage filter that has been implemented.

B. Single-stage EMI filter design

Once all constraints have been established, next step is to make an L-C map in order to enclose the possible values for main inductance and capacitance of the filter that fulfill all constraints. Attenuation and characteristic impedance are the main constraints. But, additionally, in the case of the Forward with Active Clamp, it is useful to set the resonant frequency of the filter far from the resonance between the clamp capacitor and the magnetizing inductance, in order to avoid stability problems. As a consequence, a range of frequencies has also been restricted. Figure 6 shows in yellow the L-C design space for this project.

Main values then can be set, for instance $C_f = 120\mu F$ and $L_f = 60\mu H$ fit all conditions. However, a damping network is needed in order to reduce the maximum output peak inductance. Series/parallel inductive damping and parallel capacitive damping are described in [8]. As a general conclusions, it can be said that:

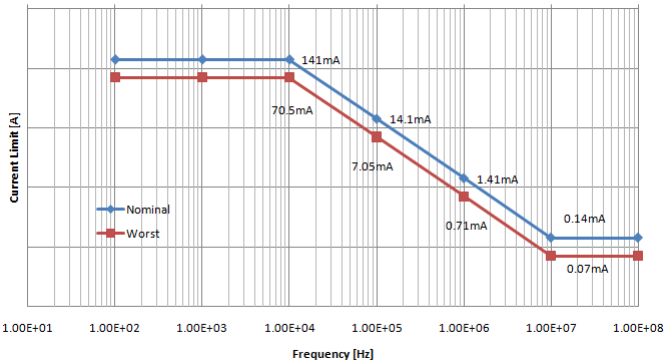

Fig. 4. Differential mode conducted emissions limit.

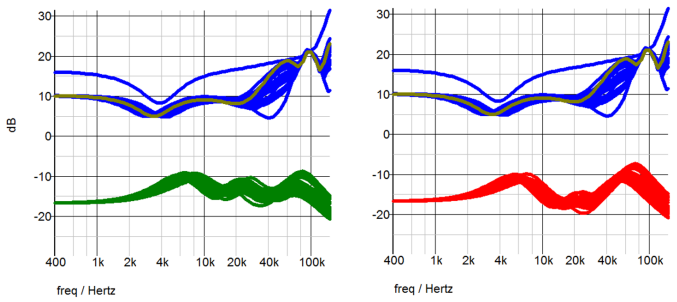

Fig. 5. Z_{out} of the filter for Range 1: *nominal Z_{in} of 1 converter in dark green, worst case in blue, Z_{out} of the filter for 1 converter in green, for 4 in red.*

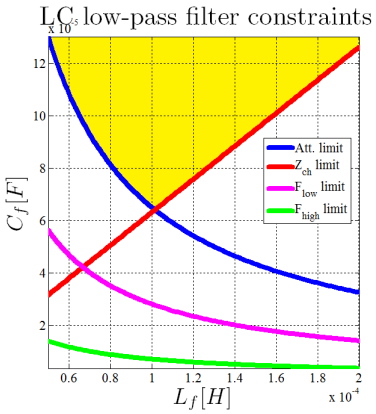

Fig. 6. Basic constraints for LC filter (attenuation limit in blue, characteristic impedance limit in red, low frequency limit in pink and high frequency limit in green). Yellow area shows possible solutions.

- Capacitive damping requires an additional capacitance, usually higher than the main one. Maximum allowed capacitance strongly restricts this kind of filter.
- Parallel inductive damping is made with an additional inductor. This is smaller than the main one since it just handles the high frequency current. However, attenuation of the filter is worsened and needs to be compensated by increasing the main C_f and L_f.
- Series inductive damping also requires an extra inductor, although losses are increased, since DC current will flow through both inductors. Nevertheless, nominal attenuation is not affected.

However, with this Single-stage approach, the size of the filter is close to the size of the power stage. A Multi-stage approach is then required.

C. Multi-stage EMI filter design

Multi-stage EMI filters offer the same performance than a Single-stage with smaller components. This is a great advantage, because the total size of the system can be reduced. On the other hand, the complexity is increased with the number of stages. Some general guidelines can be considered:

- Attenuation is higher whether filter inductance and/or filter capacitance increase, since attenuation is given by the product of both values. Total required attenuation can be distributed over all the stages in the way that resonant frequency of each one are separated.
- In a single-stage filter, the impedance of the filter inductance dominates at low frequencies and capacitance at high frequencies. But for Multi-stage filters, low frequency asymptote is equal to the series associations of all filter inductors. At high frequencies, impedance of the filter capacitor that is closest to the converter is dominant (in the case of putting several parallel modules, this dominant impedance will be equal to the parallel association of the filter capacitors of these stages).

Taking into account these considerations, architecture shown in Figure 7 is adopted for this project. For the first two stages capacitive damping is used in order to provide the big part of the attenuation. They are common, independently of the number of parallel converters. Series inductive damping has been avoided due to size and losses. Parallel inductive damping is used in the last stage in order to properly fit the output impedance of the filter and the same time that some attenuation is provided. This stage is added whenever an additional converter is connected in parallel.

Finally, the addition of this Multi-stage filter, for a single converter operation, increases the area of the converter in $300mm^2$ (21% of the total area of the converter) and the amount of losses in 2.4W (3.9% reduction of the efficiency). Then, it is important to consider the EMI aspect to provide a definitive design of the converter.

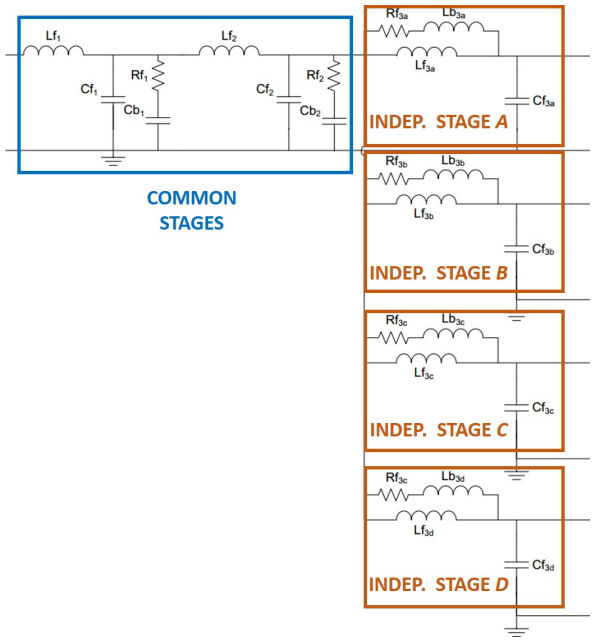

Fig. 7. Proposed multi-stage topology. From left to right, two common inductive parallel damped stages and an independent capacitive parallel damped stage.

V. Conclusions

The impact of the clamp capacitor design, the dynamic specifications and the EMI filter design on the power stage design of a Forward with Active Clamp converter for space applications has been analyzed along this work. Table III shows the differences between the preliminary and the final design.

The EMI filter has a contribution of 2.1W and damping resistor $170m$W in the total losses, what makes a reduction of the efficiency of 4%. Additionally to fulfill the deviation of the output voltage specifications under load steps, a three times higher output capacitance is required. Size of this output capacitors and the EMI filter makes a 1.6 times higher component are than for the preliminary power stage design. Finally, clamp capacitor value and core size of the transformer are modified in order to avoid the saturation during a transient.

It can be seen that all these features have a big impact on the power stage design and need to be analyzed in order to get a final design of the converter.

TABLE III
Comparison between preliminary and final design.

	PRELIMINARY	FINAL
P_{loss}	4.2W	6.6W
η	92.3%	88.4%
$Area$	890mm^2	1400mm^2
$Height$	14.3mm	16.2mm
C_{out}	20μF	60μF
C_{cl}	4.7μF	$470n$F
Transformer	RM8/I	RM10/I

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